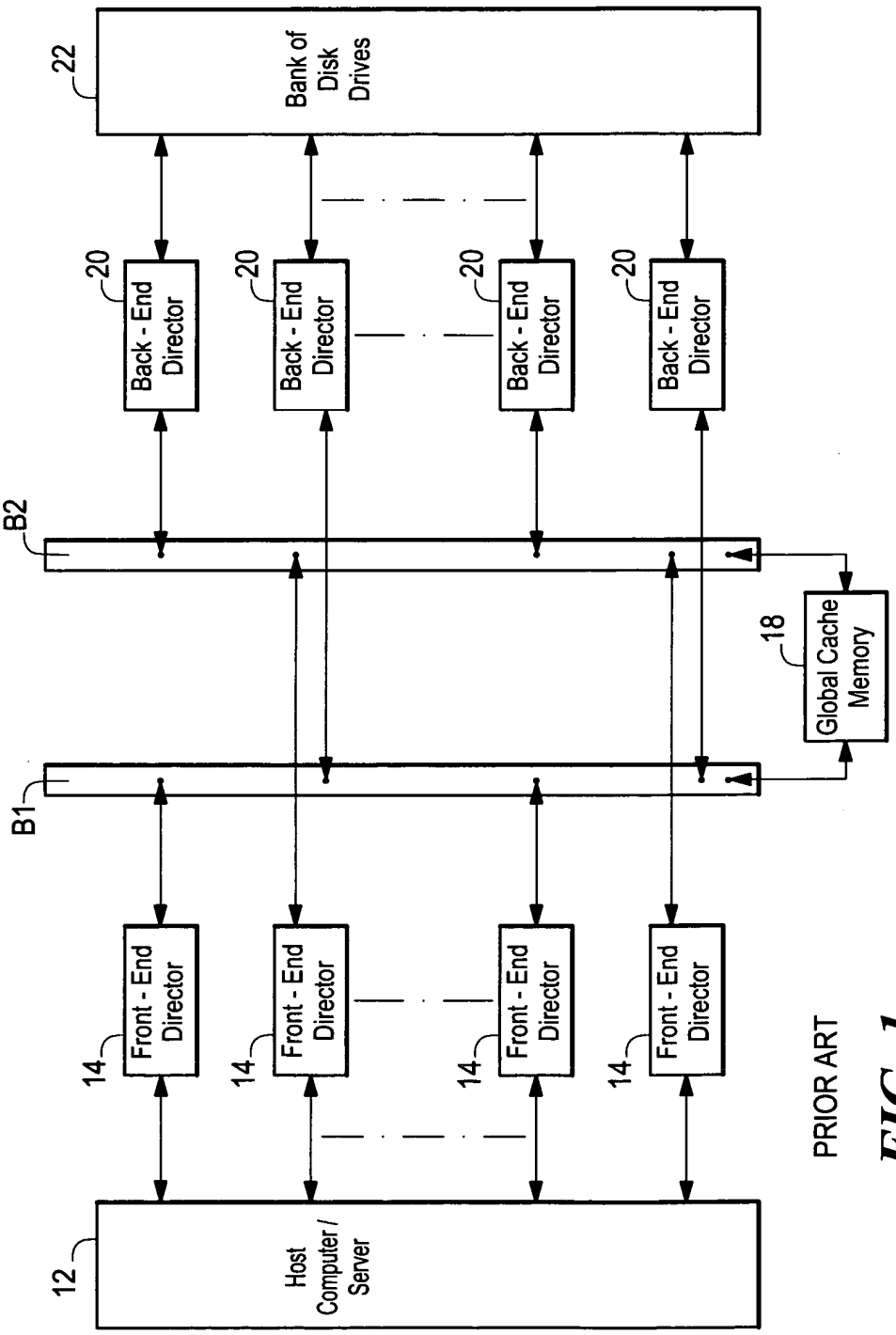


PRIOR ART

FIG. 1

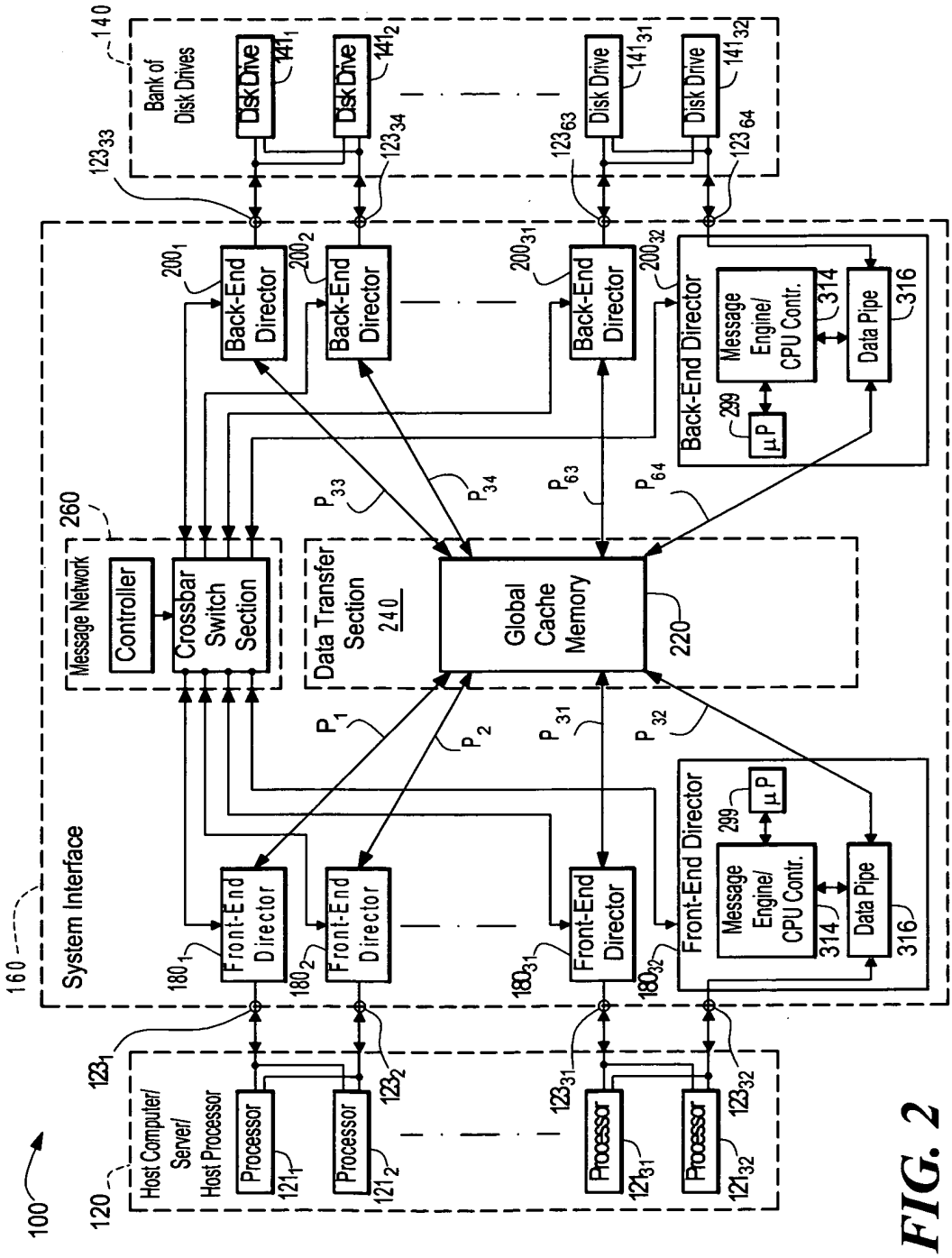


FIG. 2

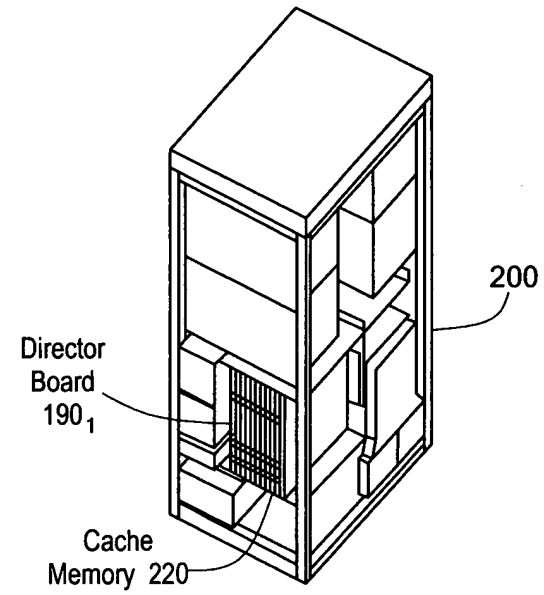


FIG. 3

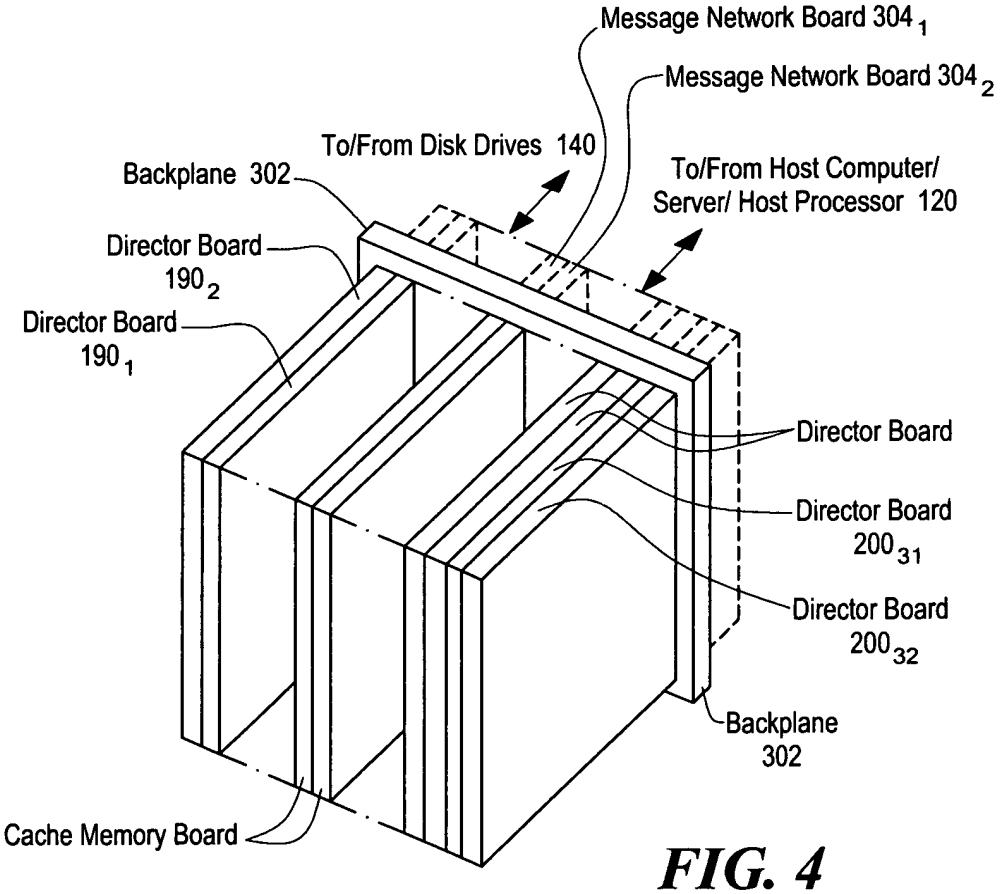
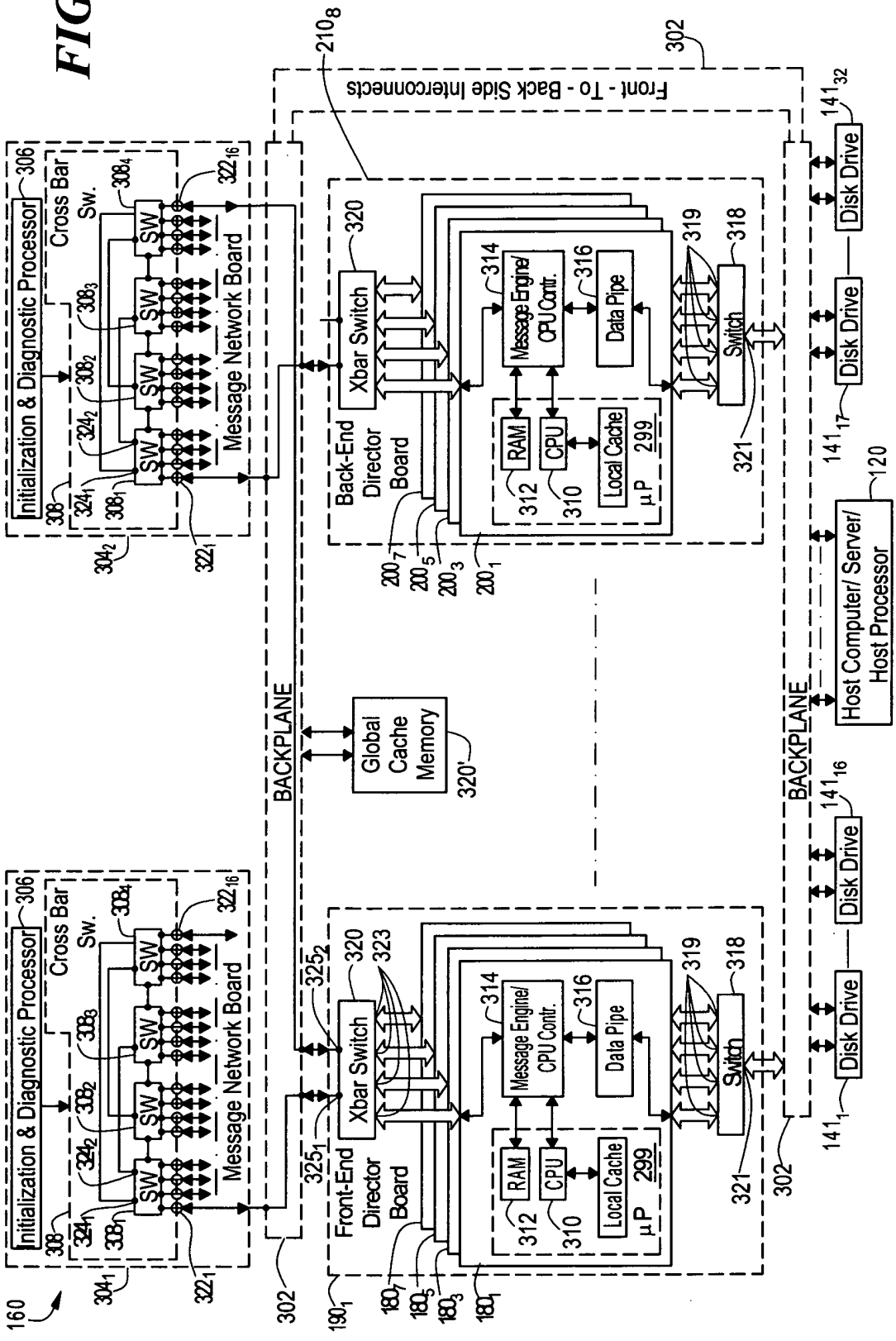


FIG. 4

FIG. 5



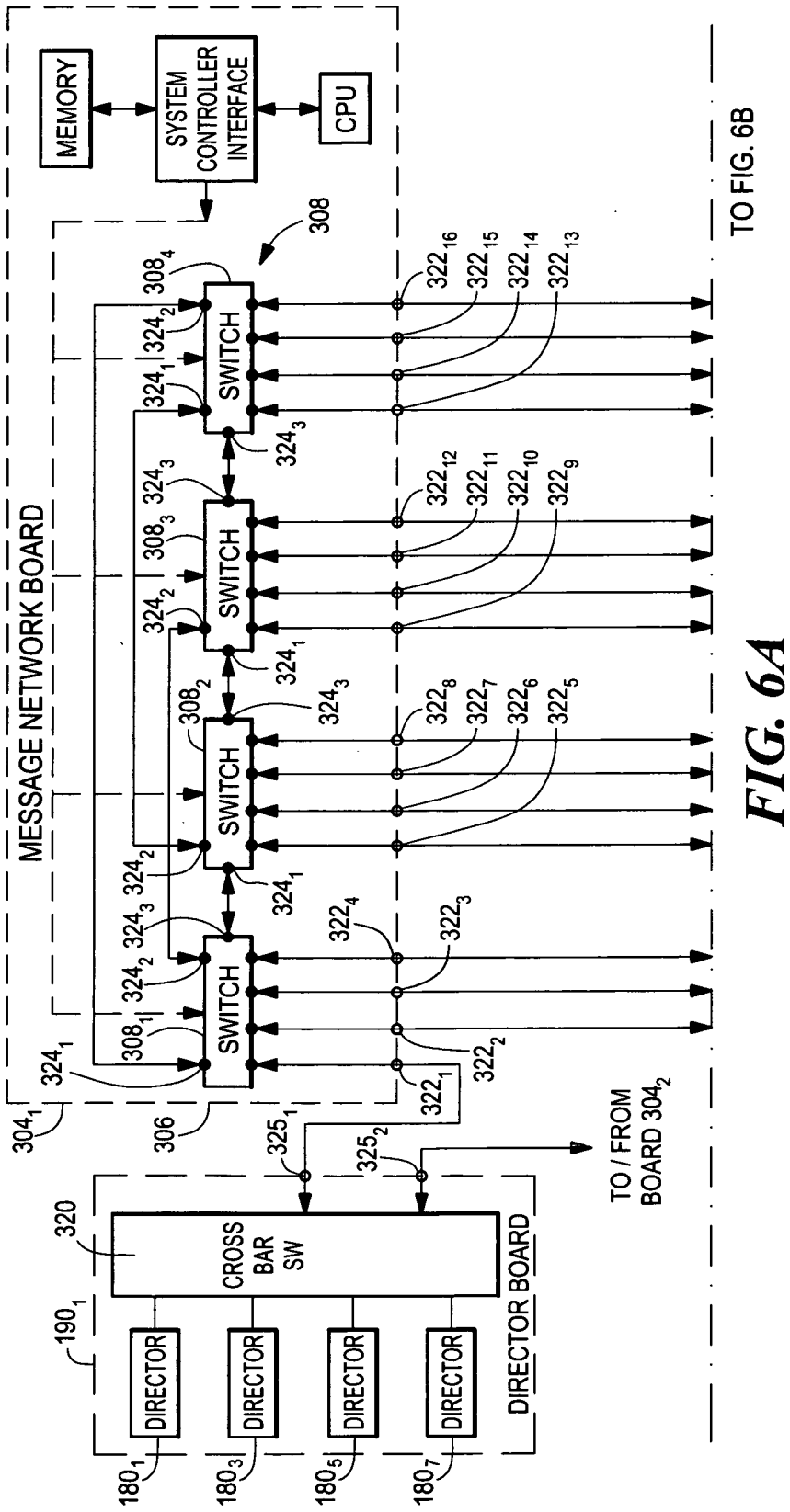


FIG. 6A

FIG. 6

FIG. 6A
FIG. 6B

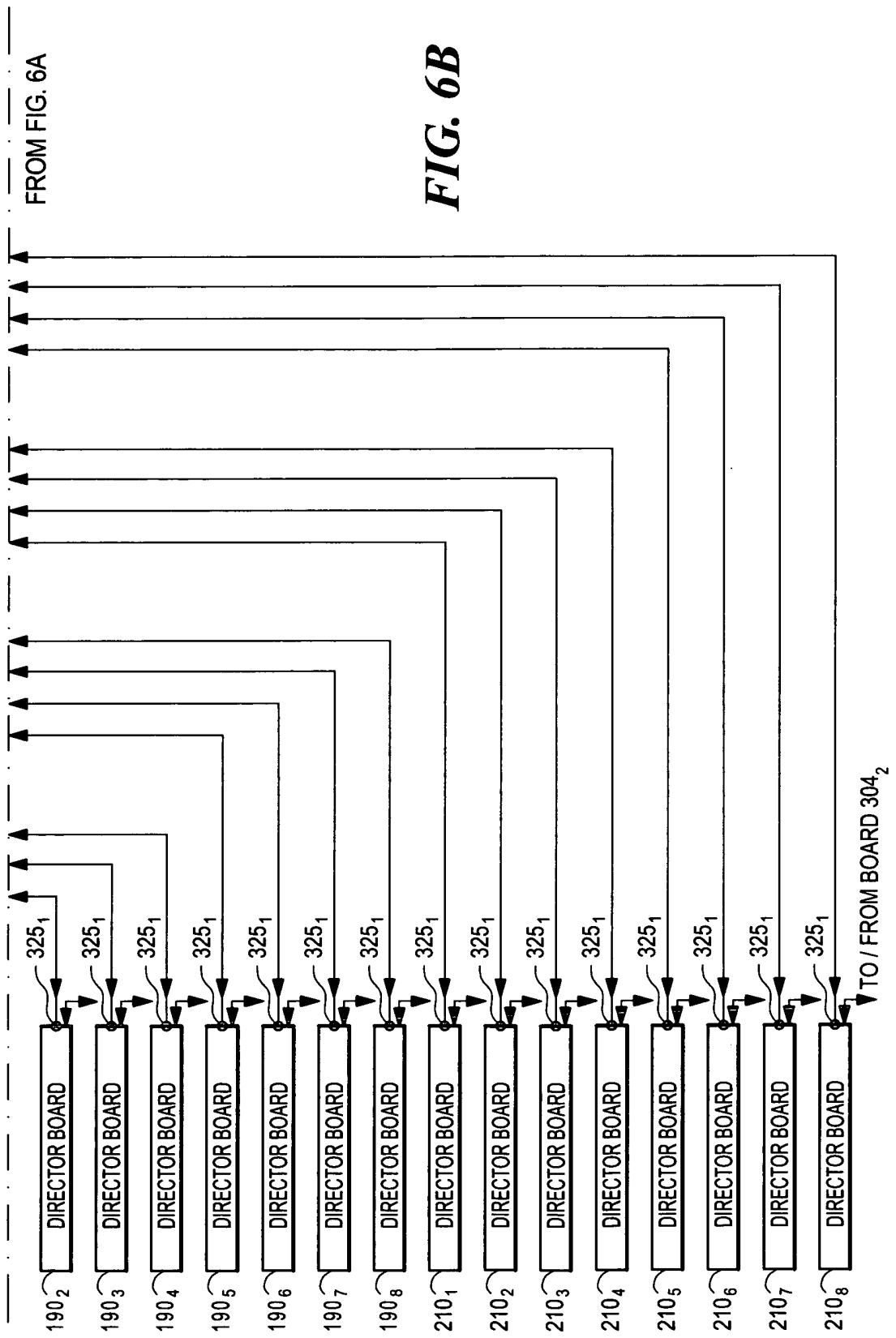


FIG. 6B

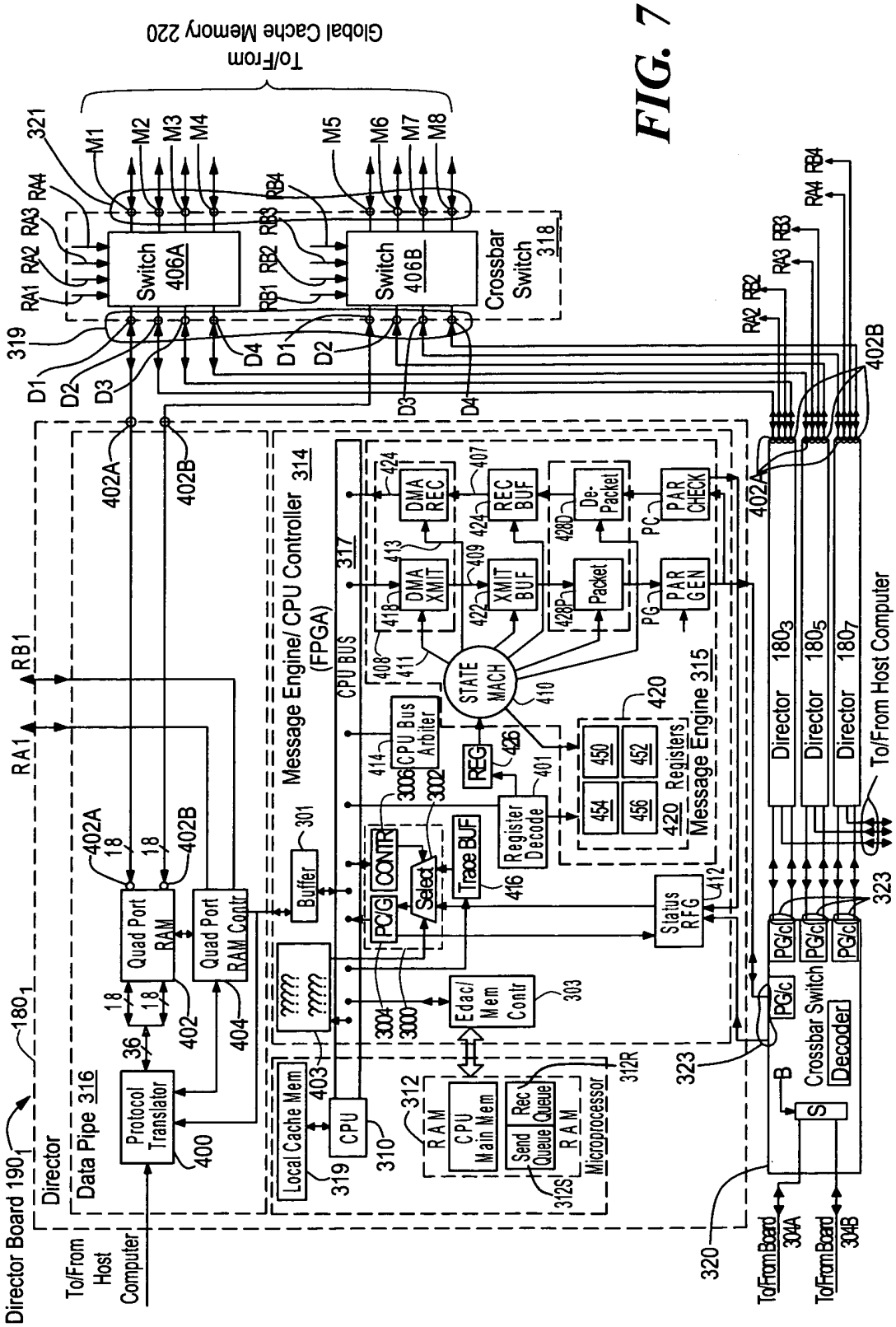


FIG. 7

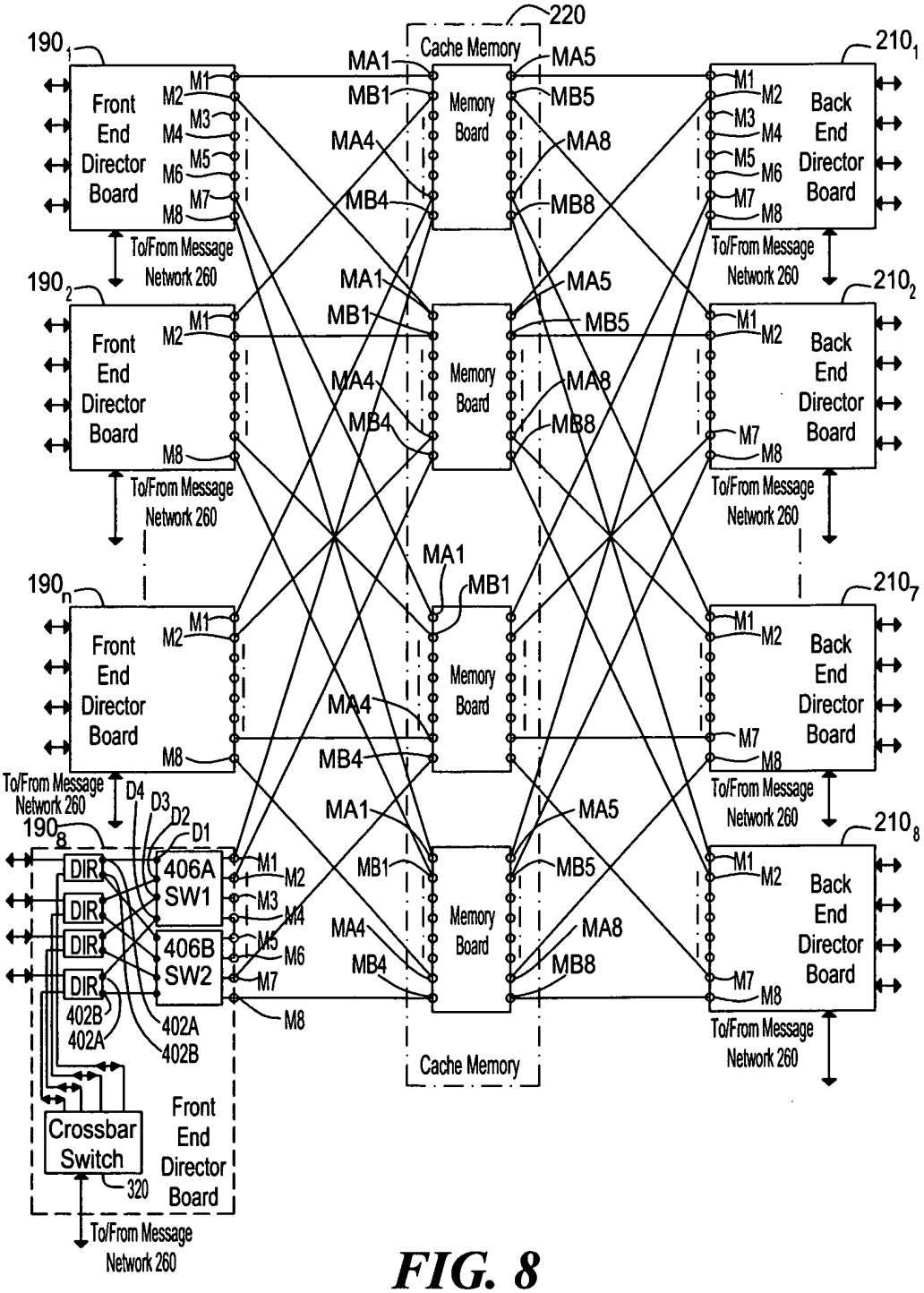


FIG. 8

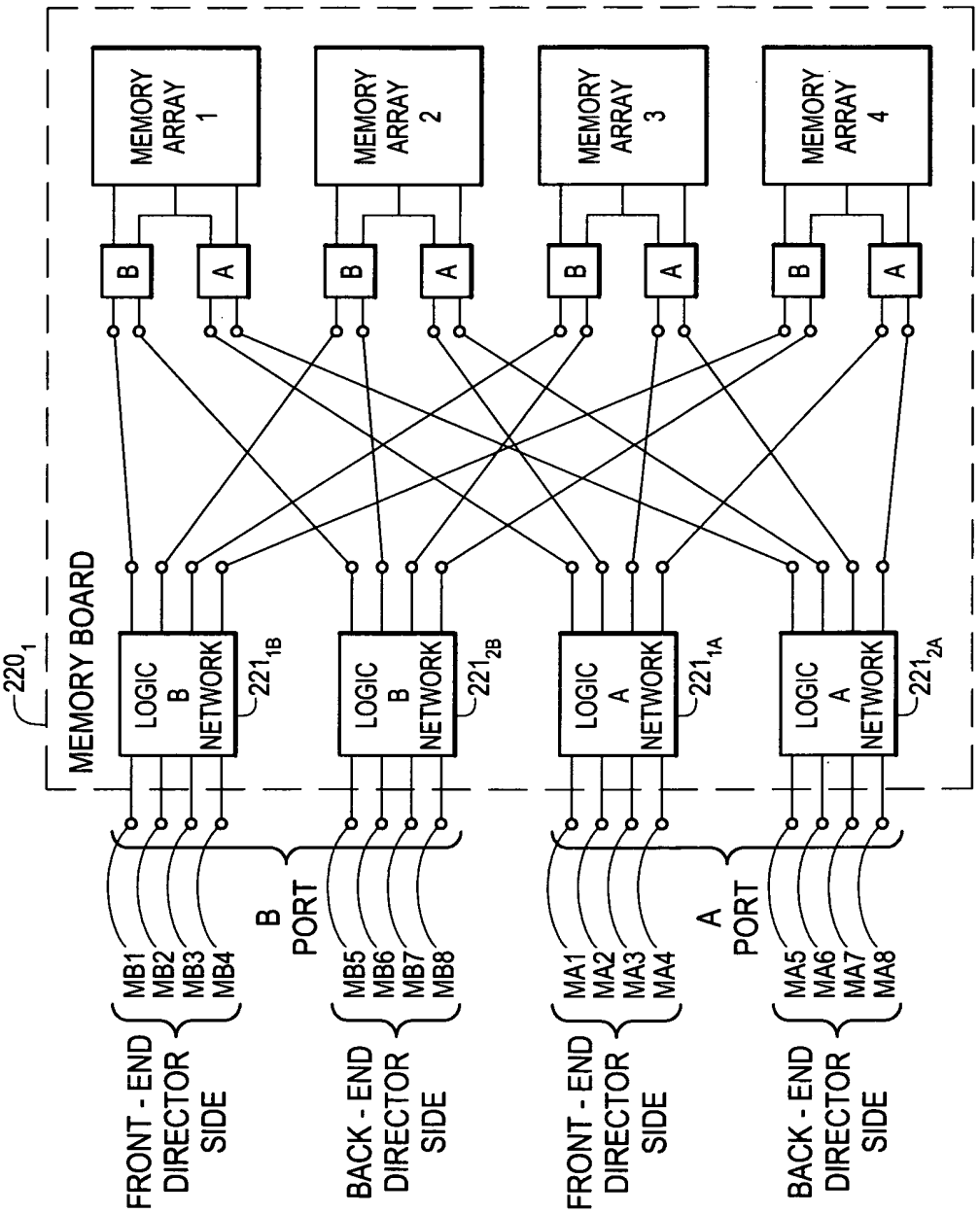


FIG. 8A

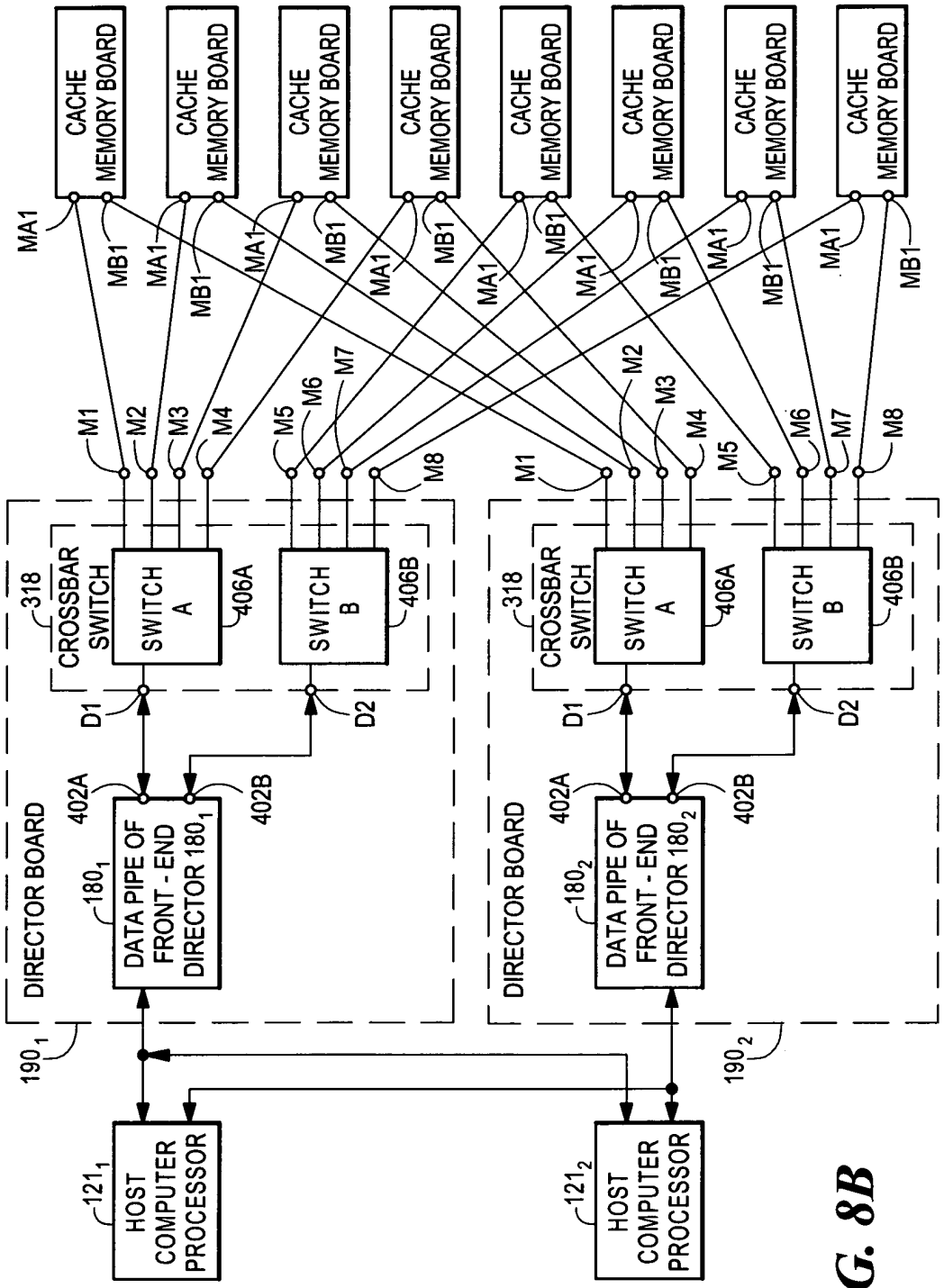


FIG. 8B

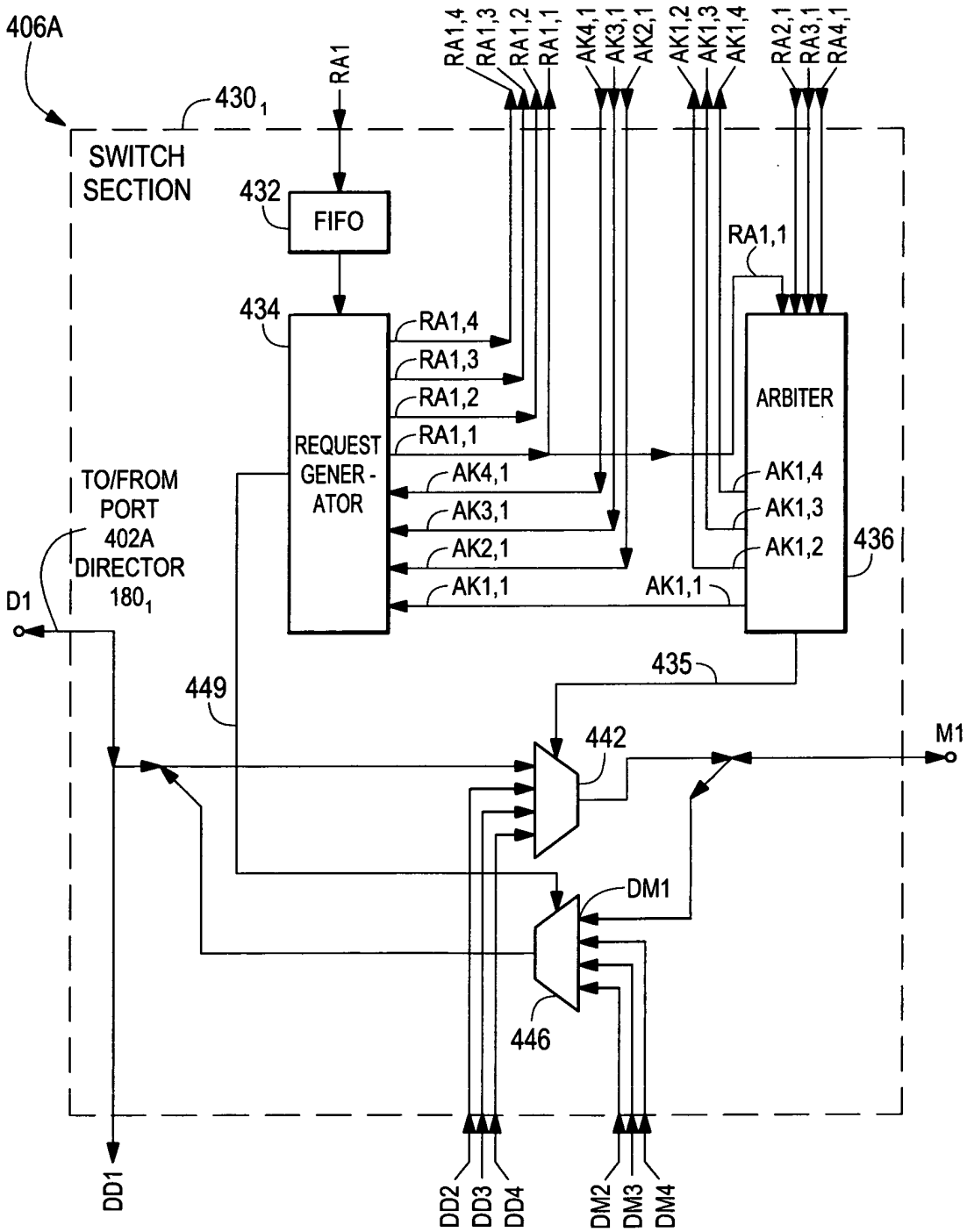


FIG. 8C-1

FIG. 8C

FIG. 8C-1
FIG. 8C-2

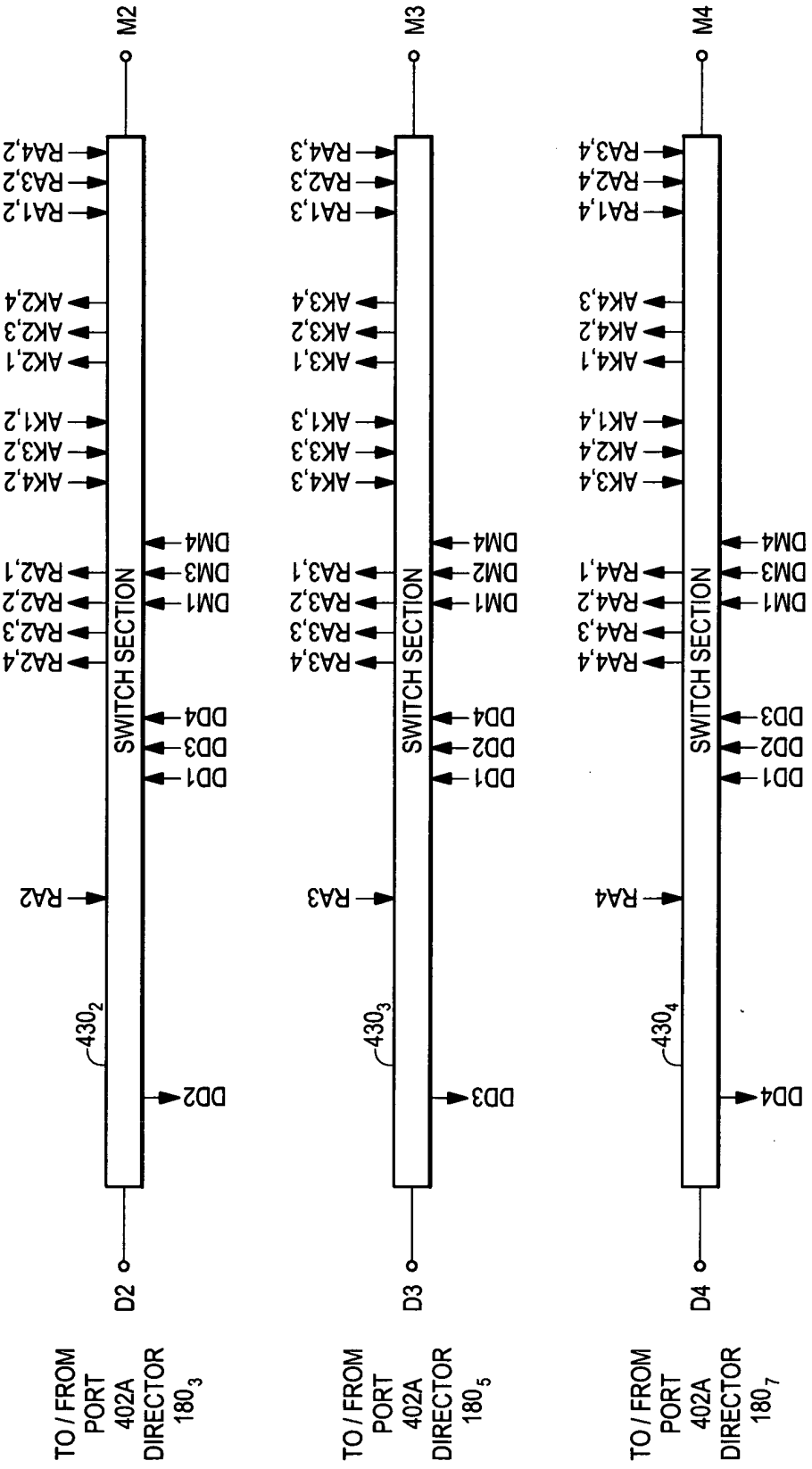


FIG. 8C-2

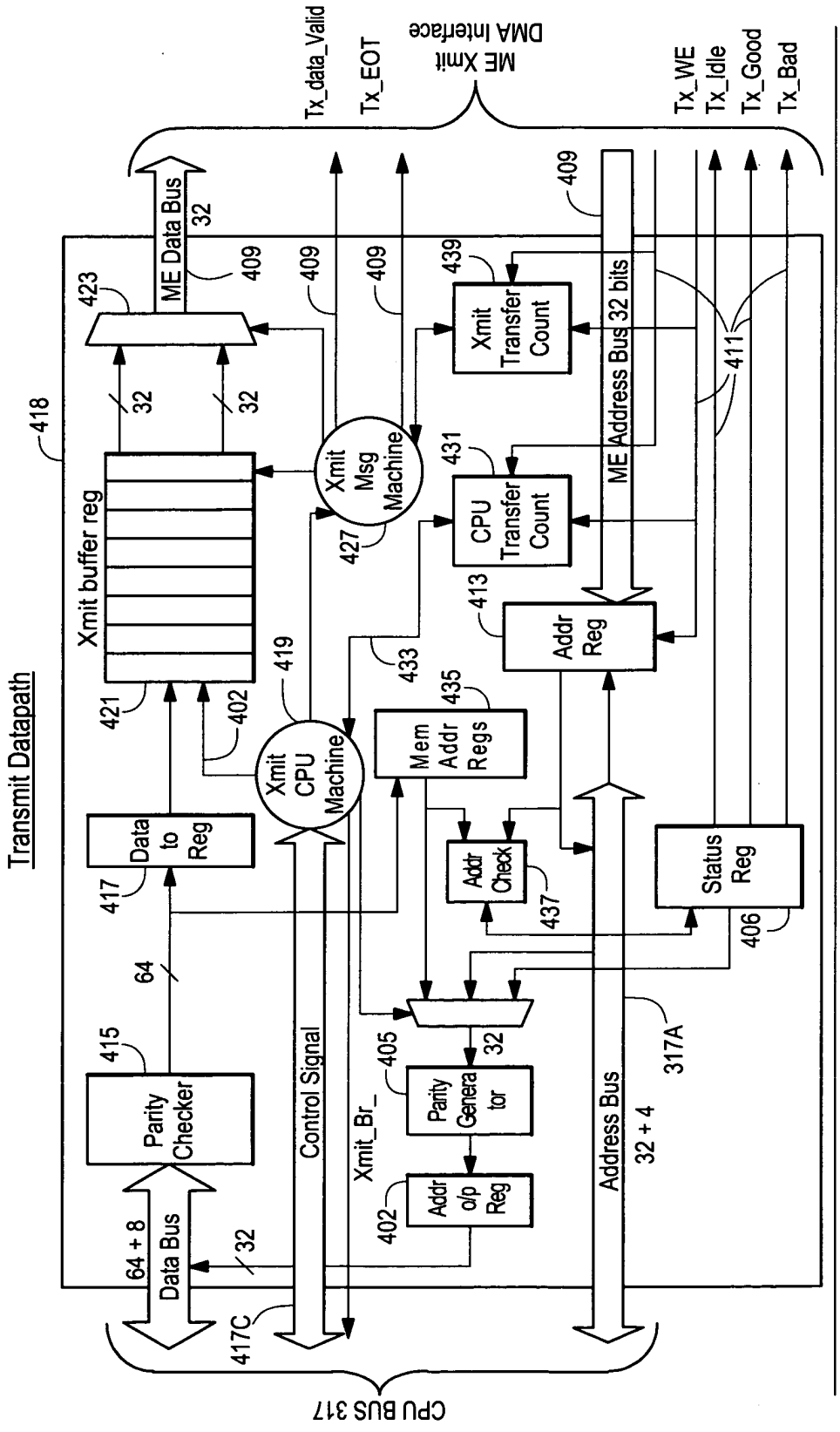


FIG. 9

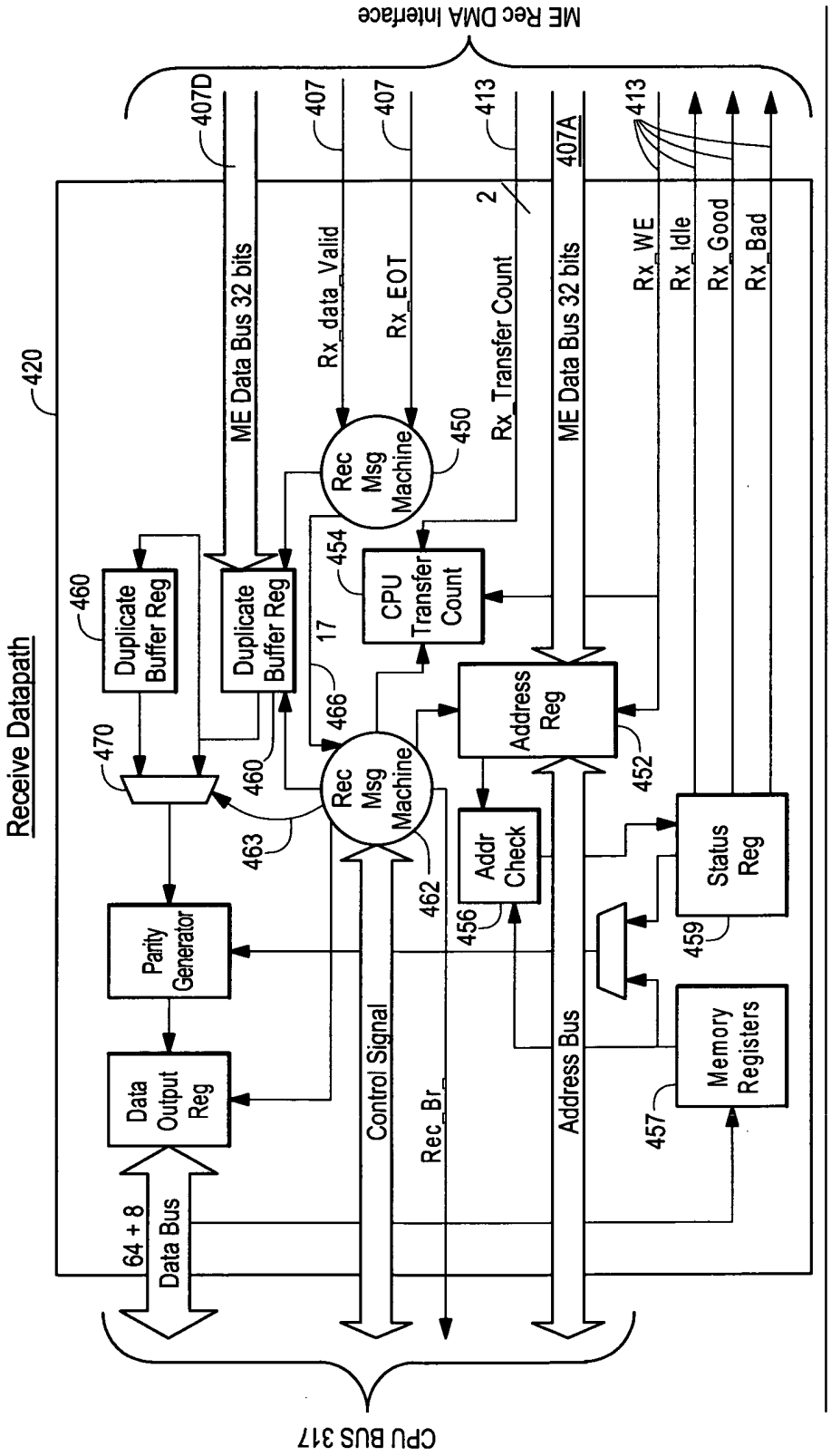


FIG. 10

FIG. 11A

FIG. 11B

FIG. 11

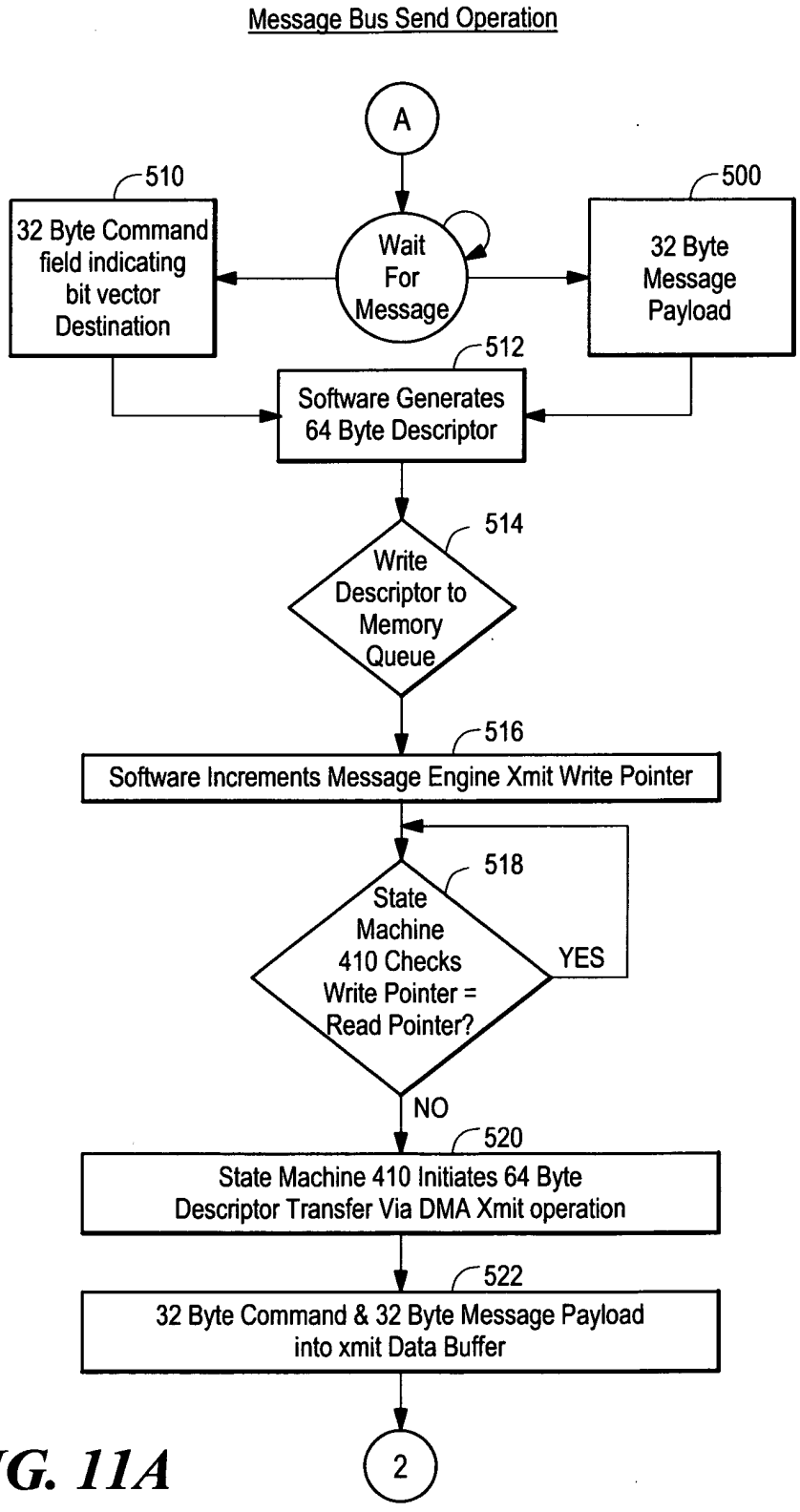


FIG. 11A

Message Bus Send Operation Continued

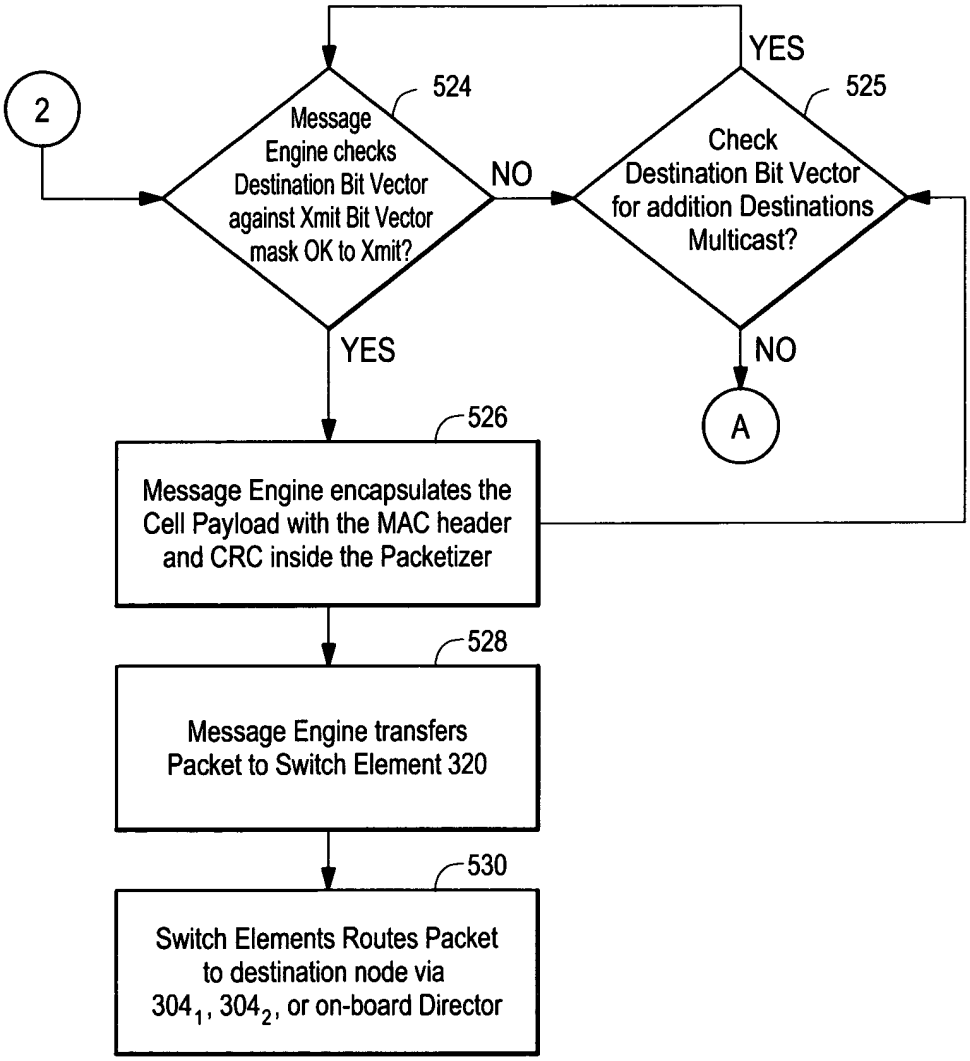


FIG. 11B

FIG. 11C

FIG. 11D

FIG. 11E

FIG. 11F

FIG. 11G

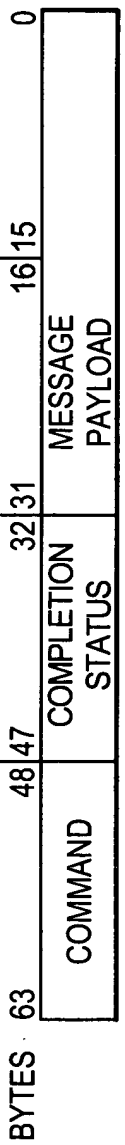


FIG. 2A

FIG. 2B

FIG. 12

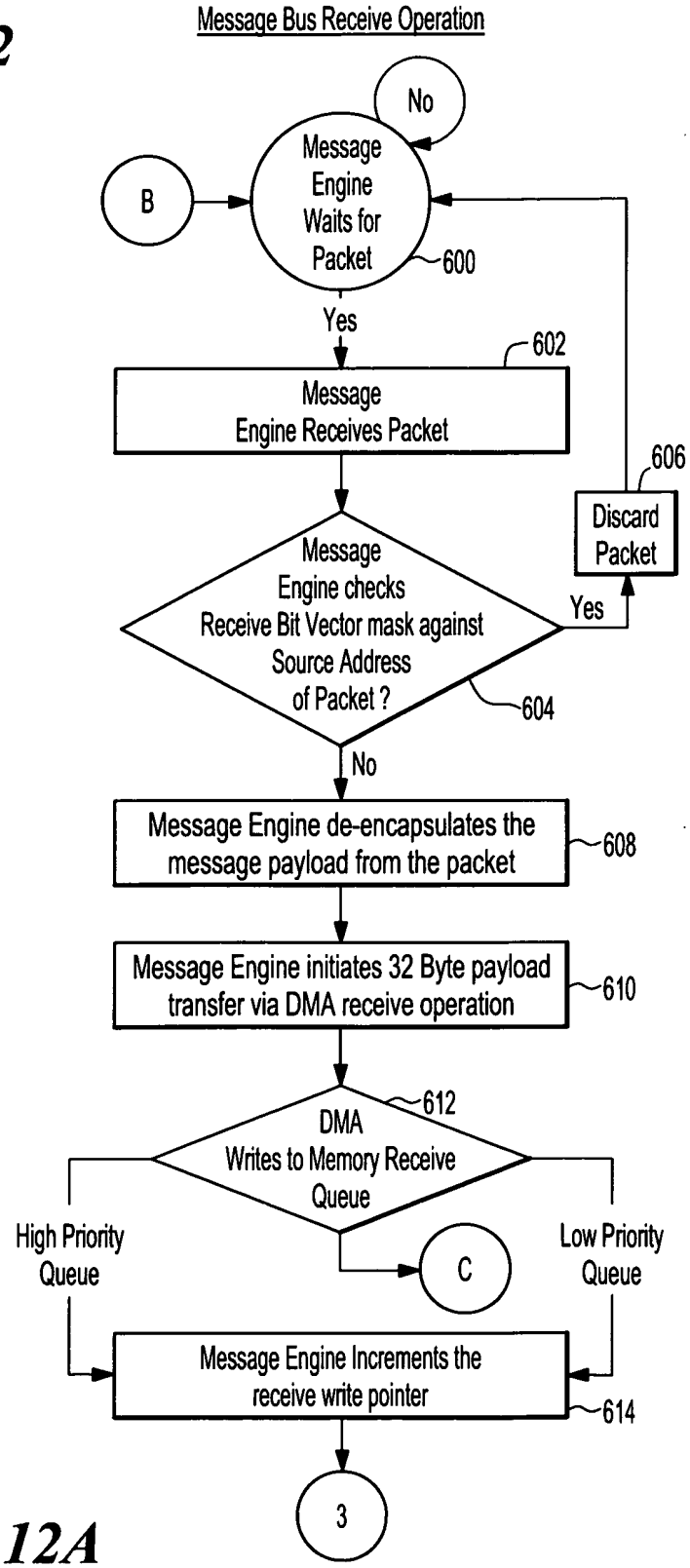


FIG. 12A

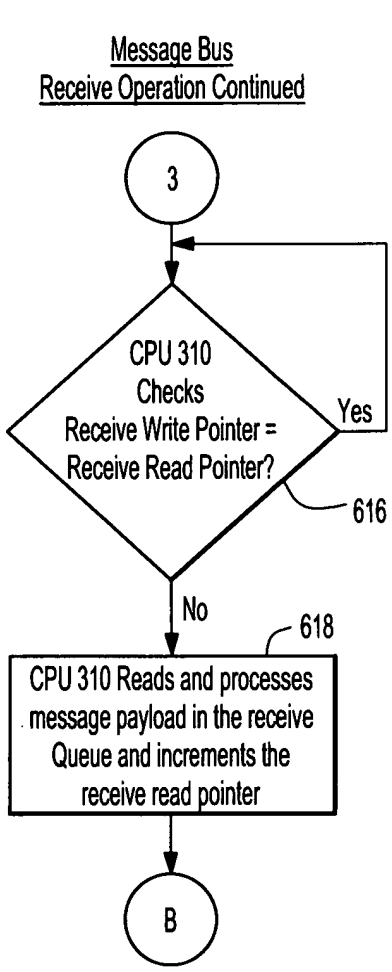


FIG. 12B

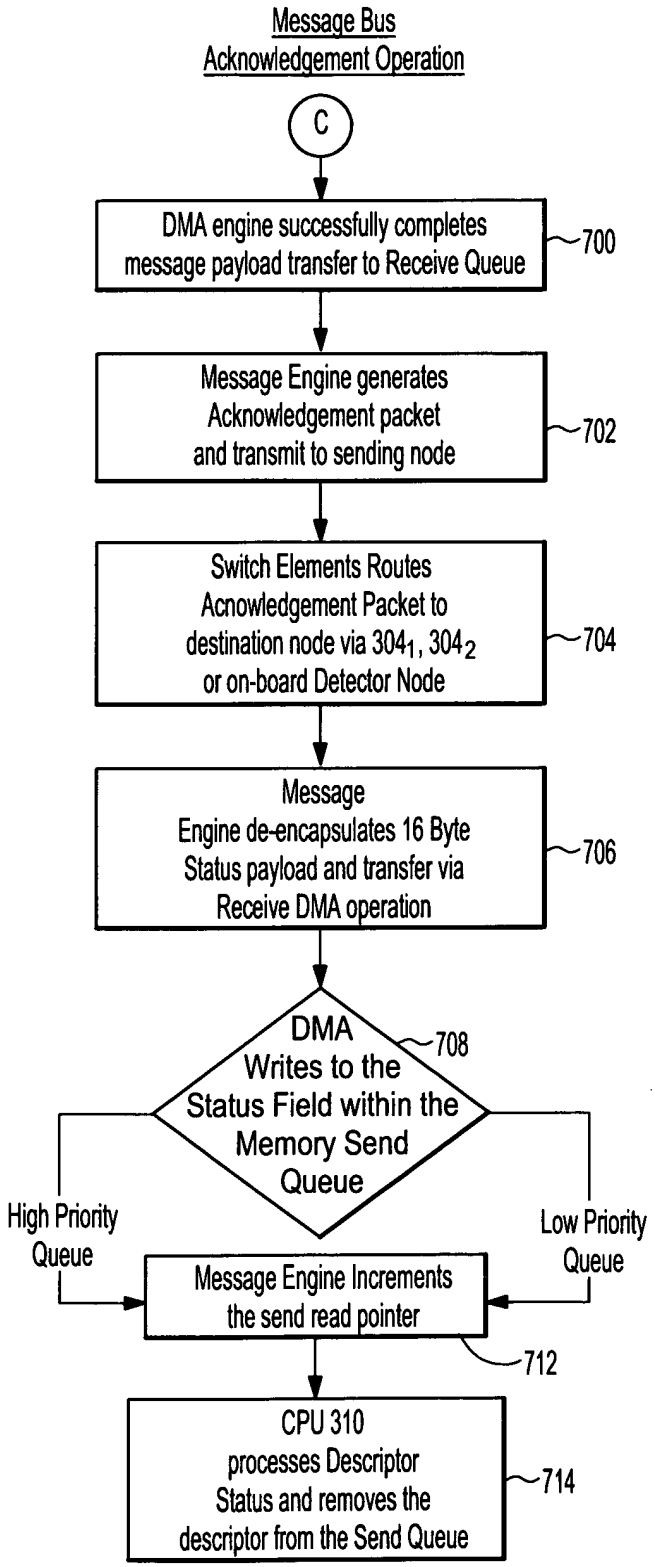


FIG. 13

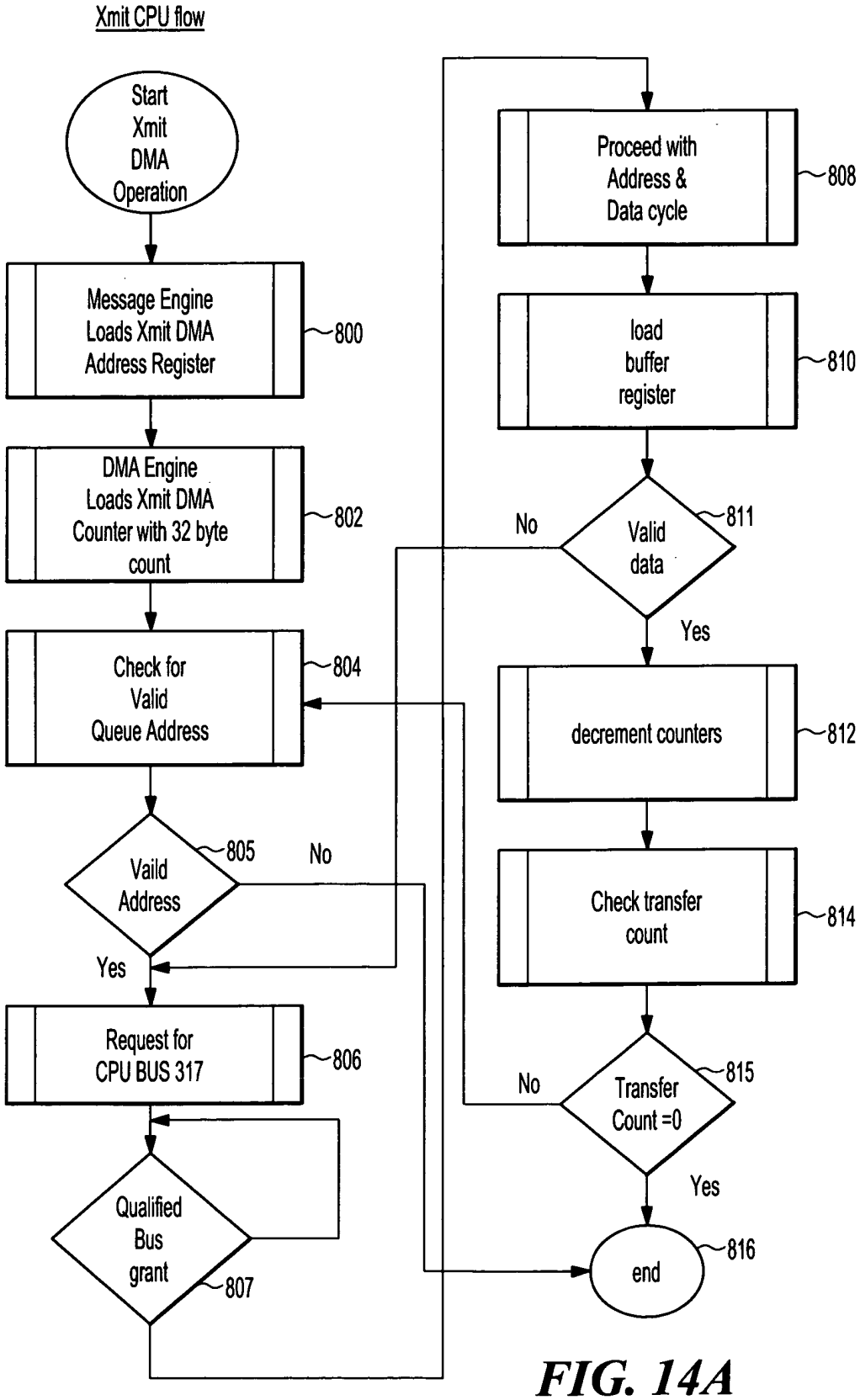


FIG. 14A

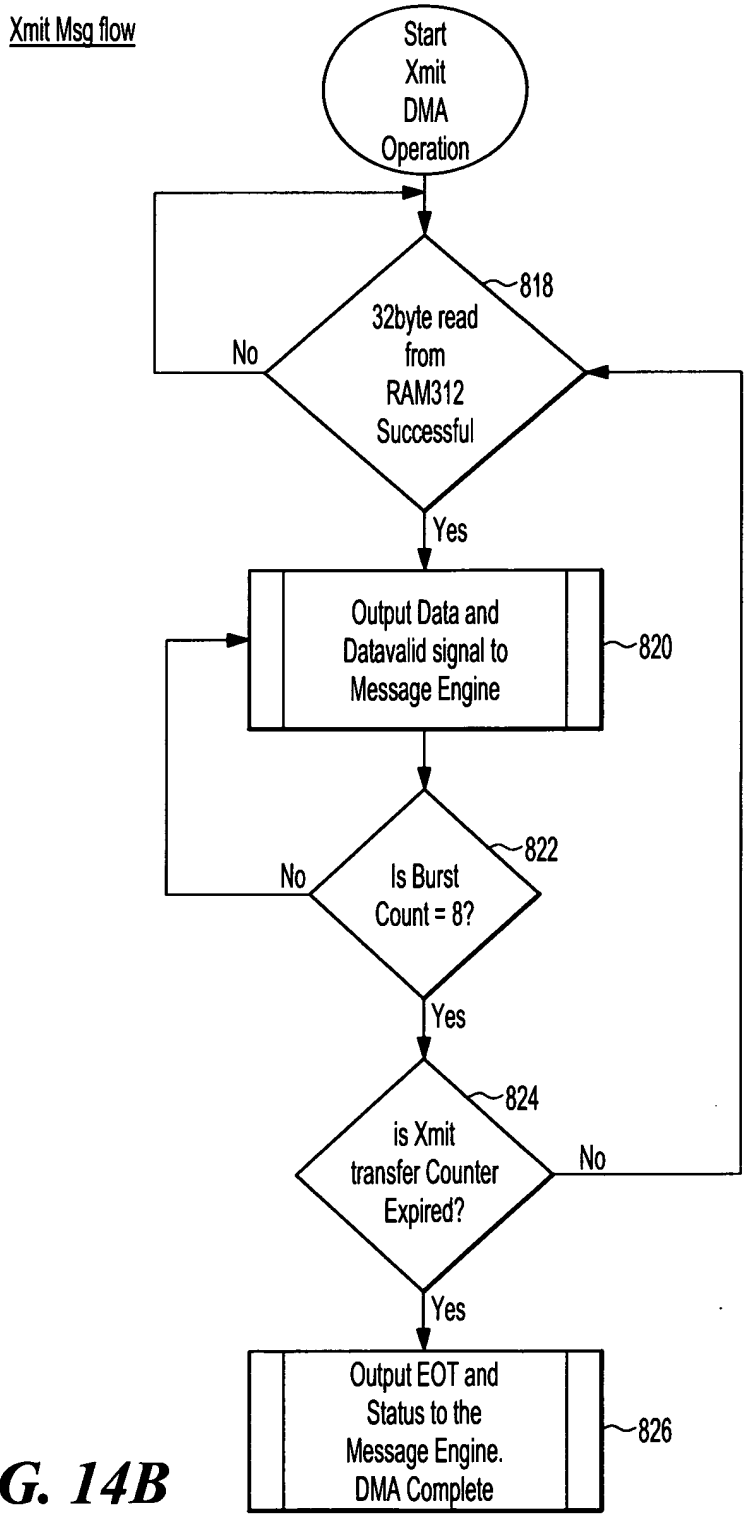


FIG. 14B

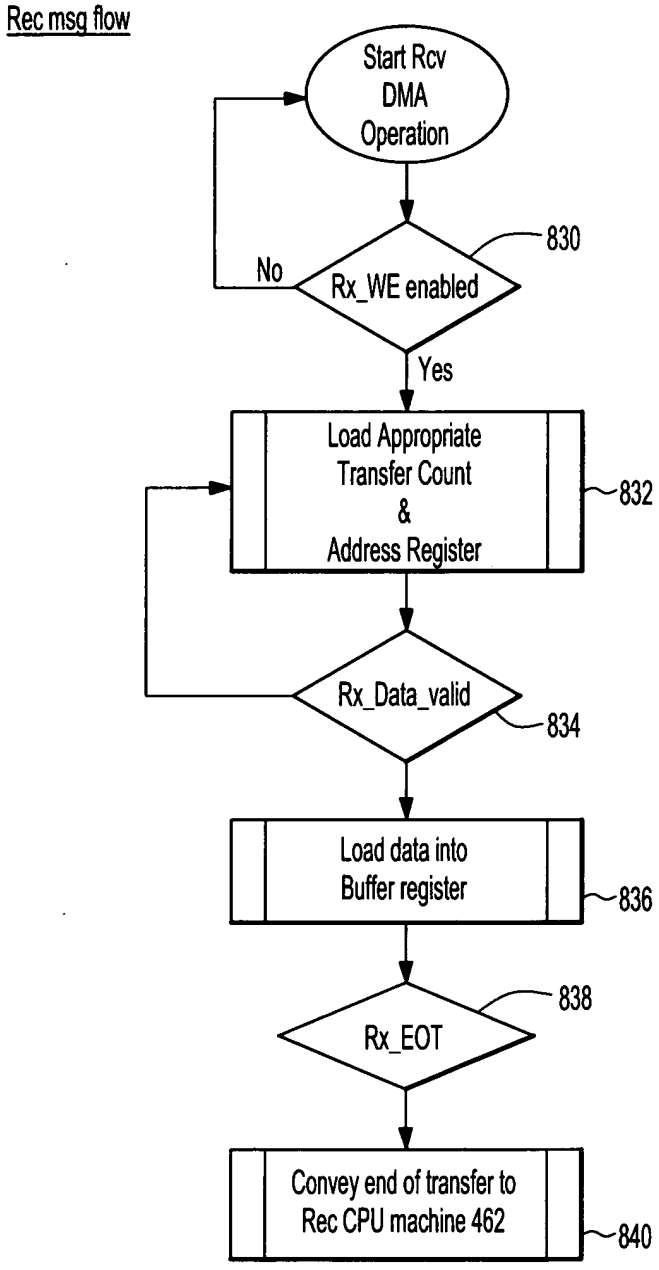


FIG. 15A

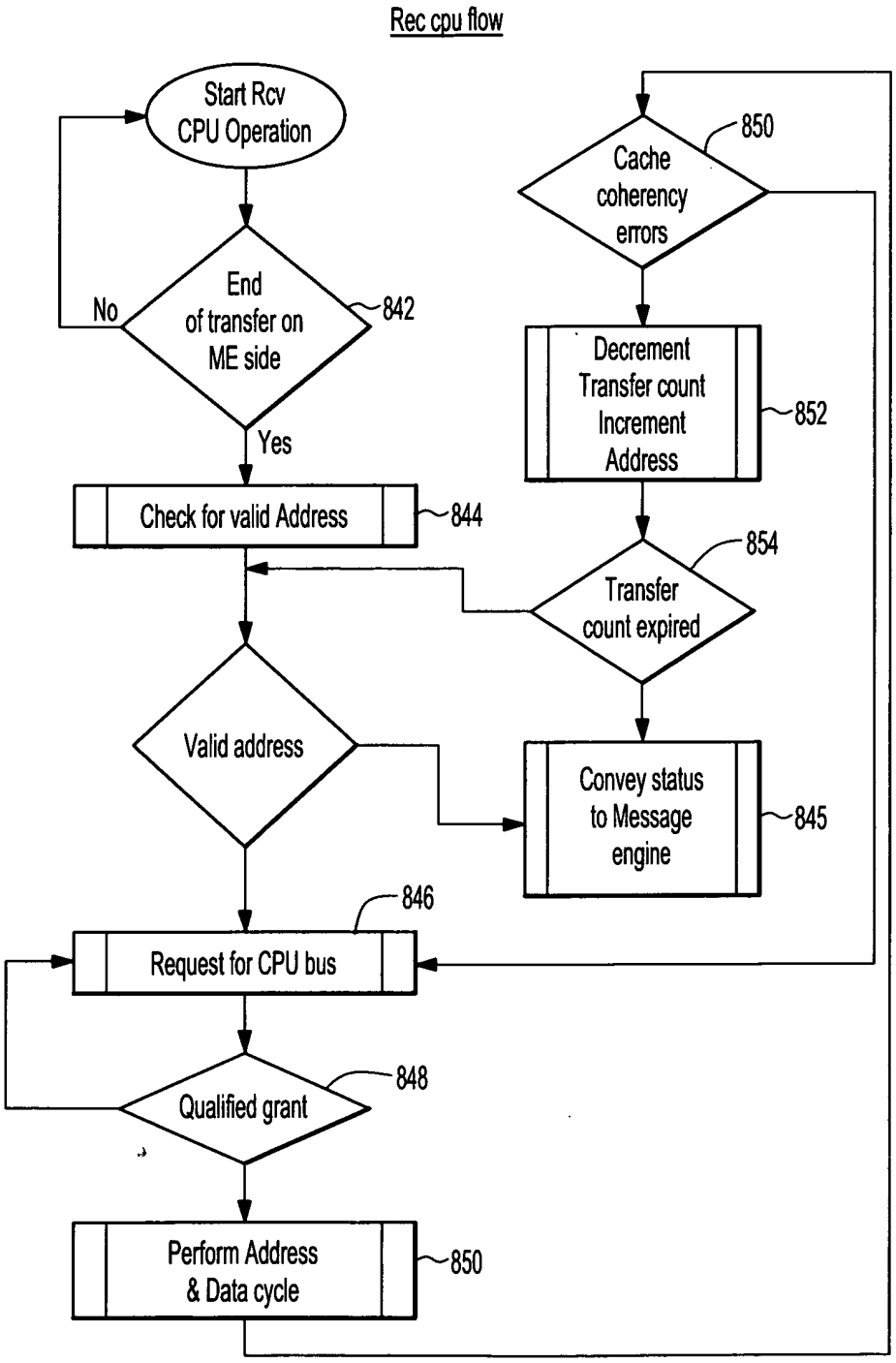


FIG. 15B

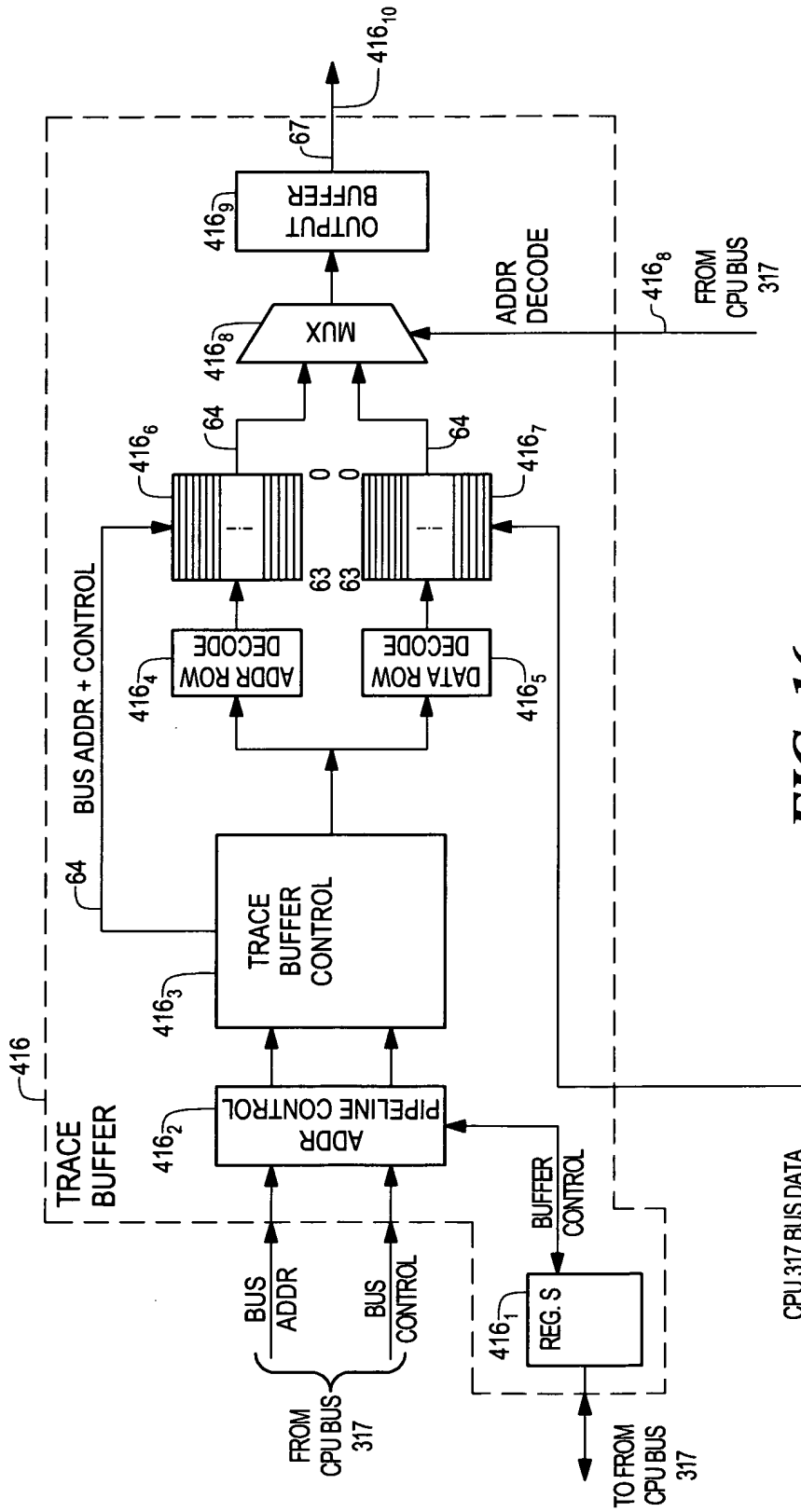


FIG. 16

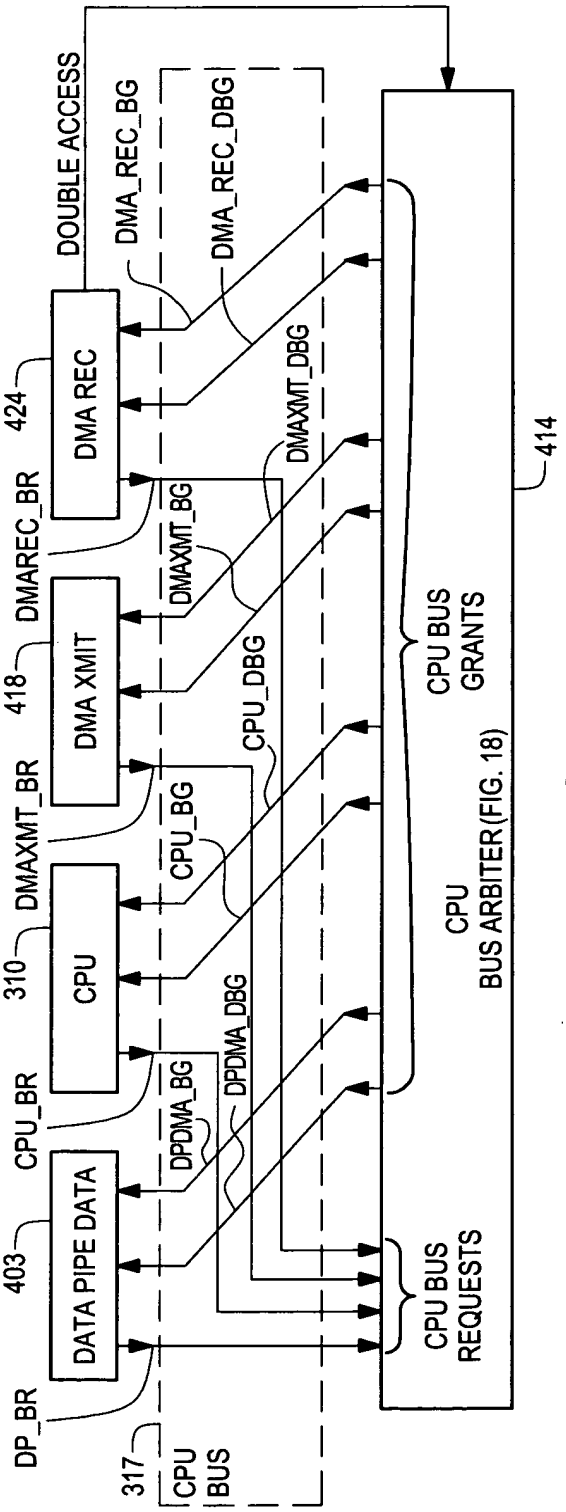


FIG. 17

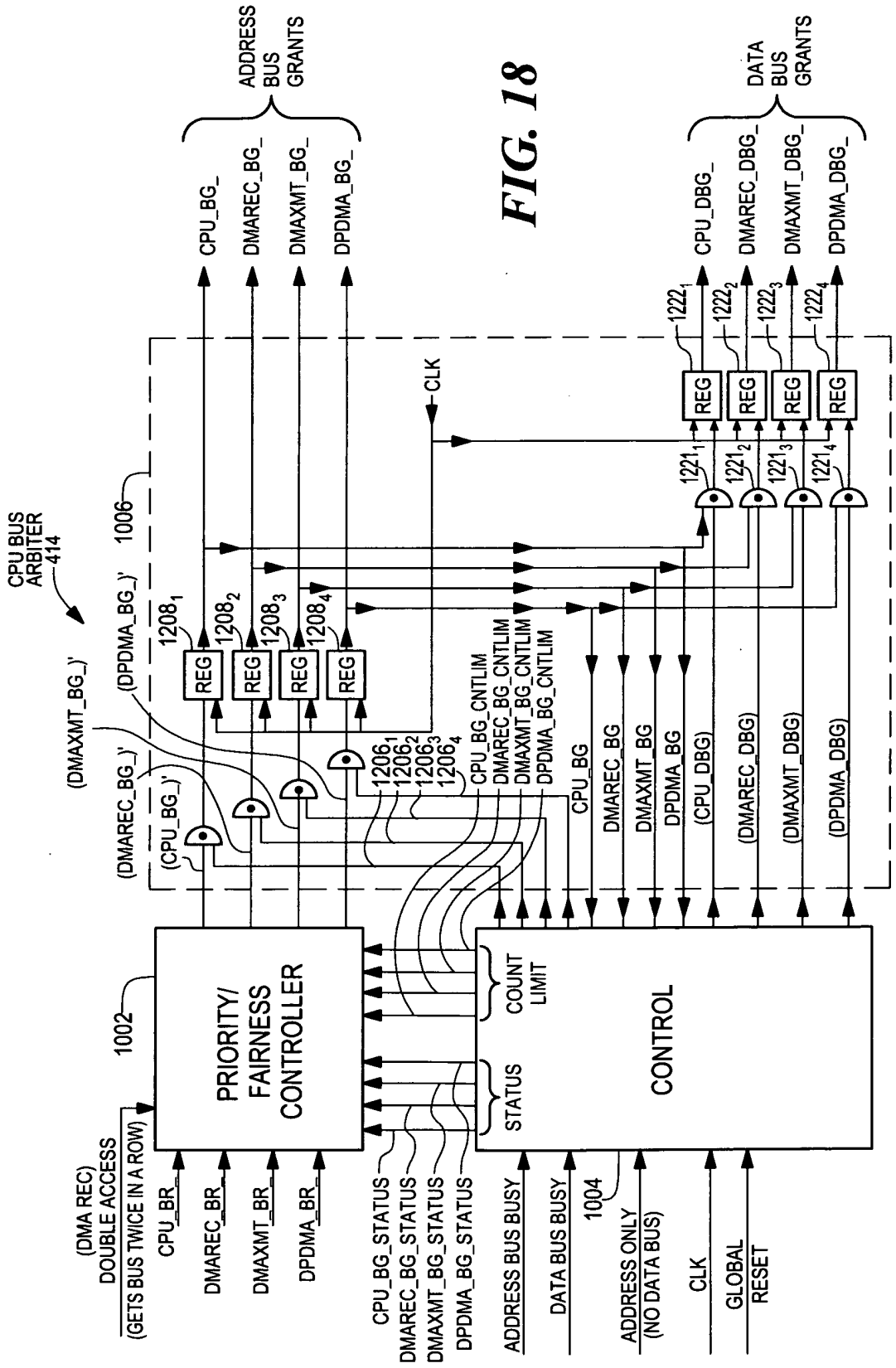


FIG. 18

POTENTIAL GRANT TO	CPU_ BR	DMAREC_ BR	DMAXMT_ BR	DPDMA_ BR	CPU_BG_ STATUS	DMAREC_BG_ STATUS	DMAXMT_BG_ STATUS	DPDMA_BG_ STATUS	CPU_BG_ CNTLIM	DMAREC_BG_ CNTLIM	DMAXMT_BG_ CNTLIM	DPDMA_BG_ CNTLIM	DOUBLE ACCESS
(CPU_BG)'	DC	0	0	0	DC	DC	DC	DC	DC	DC	DC	DC	DC
(CPU_BG)'	1	DC	DC	DC	0	DC	DC	DC	DC	0	0	0	0
(CPU_BG)'	1	DC	DC	DC	DC	DC	DC	DC	1	DC	DC	DC	0
(DMAREC_BG)'	0	1	0	0	DC	DC	DC	DC	DC	DC	DC	DC	DC
(DMAREC_BG)'	DC	1	DC	DC	DC	1	DC	DC	DC	DC	DC	0	1
(DMAREC_BG)'	0	1	DC	DC	DC	0	DC	DC	DC	DC	0	0	DC
(DMAREC_BG)'	1	1	DC	DC	1	DC	DC	DC	0	DC	0	0	DC
(DMAREC_BG)'	DC	1	DC	DC	DC	DC	DC	DC	0	1	DC	DC	DC
(DMAXMT_BG)'	0	0	1	0	DC	DC	DC	DC	DC	DC	DC	DC	DC
(DMAXMT_BG)'	0	0	1	DC	DC	DC	0	DC	DC	DC	DC	0	DC
(DMAXMT_BG)'	0	1	1	DC	DC	1	DC	DC	DC	DC	DC	0	0
(DMAXMT_BG)'	1	0	1	DC	1	DC	DC	DC	DC	DC	DC	0	DC
(DMAXMT_BG)'	DC	DC	1	DC	DC	DC	DC	DC	0	0	1	DC	0
(DPDMA_BG)'	0	0	0	1	DC	DC	DC	DC	DC	DC	DC	DC	DC
(DPDMA_BG)'	0	0	1	1	DC	DC	1	0	DC	DC	DC	DC	DC
(DPDMA_BG)'	0	1	0	1	DC	1	DC	DC	DC	DC	DC	DC	0
(DPDMA_BG)'	1	0	0	1	1	DC	DC	DC	DC	DC	DC	DC	DC
(DPDMA_BG)'	DC	DC	DC	1	DC	DC	DC	DC	0	0	0	1	0

FIG. 19

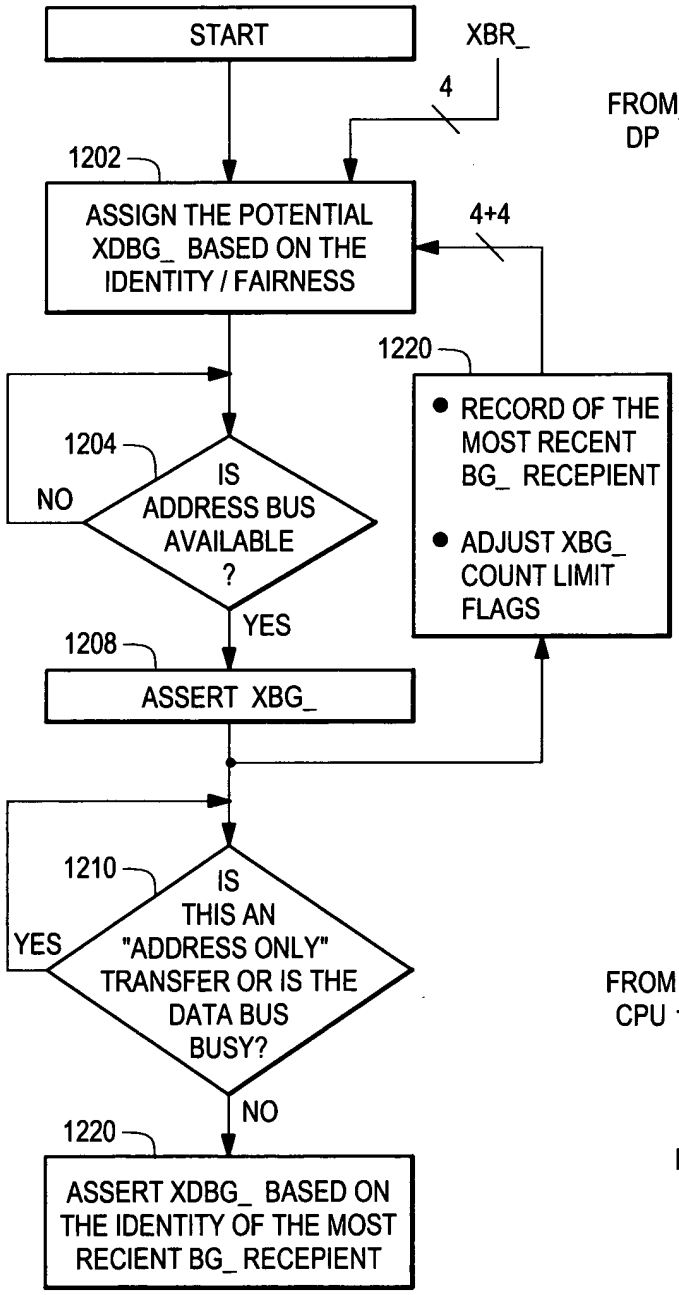


FIG. 20

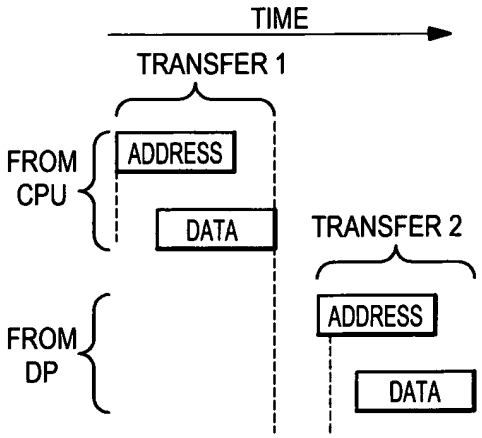


FIG. 21A

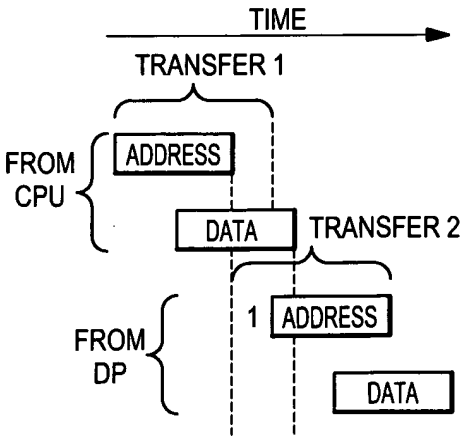


FIG. 21B

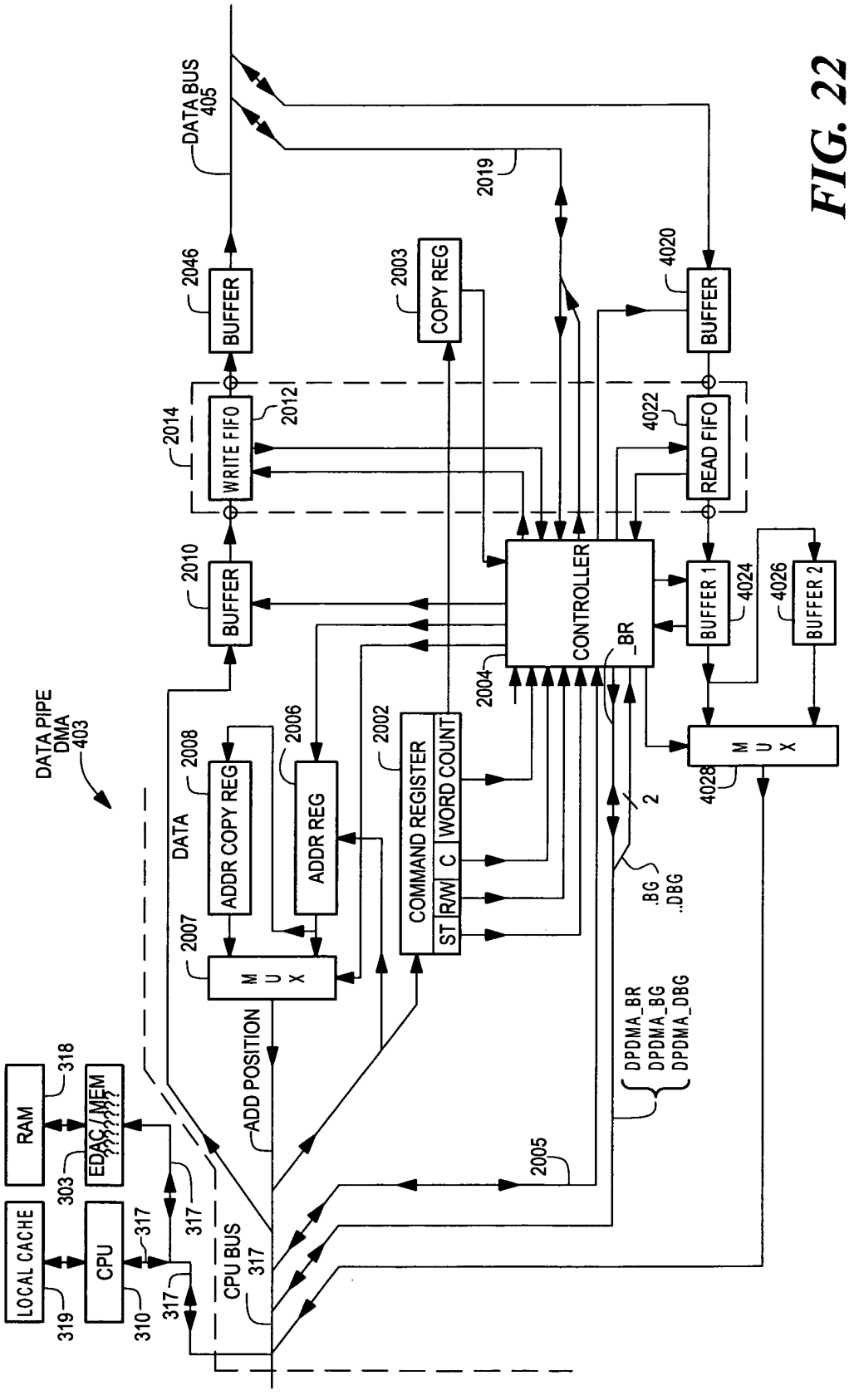


FIG. 22